What is claimed is:

1. A method of operating a memory device, comprising:

deactivating a first field-effect transistor having a first source/drain region coupled to a fuse latch input node and a second source/drain region coupled to a local bit line of a memory array of the memory device;

activating a second field-effect transistor having a first source/drain region coupled to a first potential node and a second source/drain region coupled to the fuse latch input node; and

resetting a fuse latch in response to deactivating the first field-effect transistor and activating the second field-effect transistor, wherein the fuse latch has an input coupled to the fuse latch input node and an output coupled to an output node.

2. The method of claim 1, wherein activating the second field-effect transistor occurs subsequent to deactivating the first field-effect transistor.

3. The method of claim 1, wherein activating the second field-effect transistor and deactivating the first field-effect transistor occur substantially simultaneously.

4. The method of claim 1, wherein the first field-effect transistor is an n-channel field-effect transistor and the second field-effect transistor is a p-channel field-effect transistor.

5. The method of claim 1, wherein the fuse latch includes a pair of reverse-coupled inverters.

6. The method of claim 1, wherein the method is performed automatically upon power-up of the memory device.

7. A method of operating a memory device, comprising:

deactivating a first field-effect transistor having a first source/drain region coupled to a fuse latch input node and a second source/drain region coupled to a local bit line of a memory array of the memory device;

activating a second field-effect transistor having a first source/drain region coupled to a first potential node and a second source/drain region coupled to the fuse latch input node;

resetting a fuse latch in response to deactivating the first field-effect transistor and activating the second field-effect transistor, wherein the fuse latch has an input coupled to the fuse latch input node and an output coupled to an output node; and

deactivating the second field-effect transistor subsequent to resetting the fuse latch.

8. The method of claim 7, further comprising:

activating the first field-effect transistor subsequent to deactivating the second field-effect transistor; and

driving a word line of a floating-gate memory cell coupled to the local bit line.

9. The method of claim 8, wherein driving the word line occurs while a data path associated with the local bit line is unselected.

10. The method of claim 8, further comprising:

latching a data value of the floating-gate memory cell in the fuse latch.

11. The method of claim 8, further comprising:

reading the data value of the floating-gate memory cell using a data path of the memory array.

12. The method of claim 8, further comprising:
writing a data value to the floating-gate memory cell using a data path of the memory array.

13. The method of claim 7, wherein the method is performed automatically upon power-up of the memory device.

14. A method of operating a memory device, comprising:
generating a first control signal indicative of whether it is desired to set a fuse latch of a first fuse circuit to some fuse data value without regard to a data value of a floating-gate memory cell associated with the first fuse circuit;
generating a second control signal indicative of the fuse data value;
deactivating a first field-effect transistor and a second field-effect transistor when the first control signal has a first logic level, wherein the first field-effect transistor is coupled between a first potential node and an output node of the fuse circuit, and wherein the second field-effect transistor is coupled between a second potential node and the output node of the fuse circuit; and
selectively activating either the first field-effect transistor or the second field-effect transistor in response to a logic level of the second control signal when the first control signal has a second logic level.

15. The method of claim 14, wherein generating the first control signal comprises combining a plurality of address match signals in a NAND gate and combining an output of the NAND gate with an enable signal in a NOR gate.

16. The method of claim 15, further comprising:
combining the output of the NAND gate with a second enable signal in a second NOR gate, thereby generating a third control signal; and
applying the third control signal to a second fuse circuit.

17. A method of operating a memory device, comprising:
programming a floating-gate memory cell to a cell data value using a data path of the memory device; and
transferring the cell data value to a fuse latch.

18. The method of claim 17, further comprising:
resetting the fuse latch to an initial fuse data value prior to transferring the cell data value to the fuse latch.

19. The method of claim 18, wherein resetting the fuse latch further comprises:
isolating the floating-gate memory cell from an input of the fuse latch; and
applying a supply potential to the input of the fuse latch.

20. The method of claim 19, wherein transferring the cell data value to the fuse latch further comprises:
isolating the input of the fuse latch from the supply potential;
coupling the floating-gate memory cell to the input of the fuse latch; and
applying a read voltage to a gate of the floating-gate memory cell.

21. The method of claim 20, wherein the read voltage has a potential level sufficient to activate the floating-gate memory cell if it is erased, but insufficient to fully activate the floating-gate memory cell if it is programmed.

22. The method of claim 17, further comprising:
setting the fuse latch to a data value without regard to, and without disturbing the data value of, the floating-gate transistor.

23. The method of claim 17, wherein the method is performed automatically upon power-up of the memory device.